CLAIMS

1. An integrated circuit comprising:

a register file bit comprising:

a first latch having a data input and a data output;

a second latch having a data input and a data output;

a feedback path from the data output of the second latch to the data input of the first latch; and

a context switch mechanism that causes the data on the data output of the first latch to be written to the second latch, and that causes the data on the data output of the second latch to be written to the first latch.

2. The integrated circuit of claim 1 wherein the context switch mechanism comprises a swap signal coupled to the first latch.

3. The integrated circuit of claim 1 wherein the context switch mechanism comprises a delay element between the data output of the first latch and the data input of the second latch.

4. The integrated circuit of claim 1 wherein the context switch mechanism comprises a delay element in the feedback path.

5. The integrated circuit of claim 1 wherein the context switch mechanism comprises at least one clock signal that latches data on the data input of the first latch to the data output of the first latch and at least one clock signal that latches data on the data input of the second latch to the data output of the second latch.

6. The integrated circuit of claim 1 further comprising a plurality of write ports on the data input of the first latch.

7. The integrated circuit of claim 1 further comprising a plurality of read ports on the data output of the first latch.

8. An integrated circuit comprising:

a register file bit comprising:

a first latch having a data input with a plurality of write ports and a data output with a plurality of read ports;

a second latch having a data input and a data output, wherein the data output of the first latch is coupled to the data input of the second latch through a first delay element;

a feedback path from the data output of the second latch to the data input of the first latch, the feedback path including a second delay element; and

a swap signal coupled to the first latch that causes the data on the data output of the first latch to be written to the second latch, and that causes the data on the data output of the second latch to be written to the first latch.

9. An integrated circuit comprising:

a register file bit comprising:

a primary latch having a data input and a data output;

a plurality of secondary latches each having a data input and a data output;

a feedback path from the data output of the plurality of secondary latches to the data input of the first latch, the feedback path including a data selection mechanism for selecting one data output from the plurality of secondary latches to feed back to the data input of the first latch; and

a context switch mechanism that causes the data on the data output of the primary latch to be written to a selected one of the plurality of secondary latches, and that causes the data on the data output of the selected one secondary latch to be written to the primary latch.

10. The integrated circuit of claim 9 wherein the context switch mechanism comprises a swap signal coupled to the primary latch.

11. The integrated circuit of claim 9 wherein the context switch mechanism comprises a delay element between the data output of the primary latch and the data inputs of the plurality of secondary latches.

12. The integrated circuit of claim 9 wherein the context switch mechanism comprises a delay element in the feedback path.

13. The integrated circuit of claim 9 wherein the context switch mechanism comprises at least one clock signal that latches data on the data input of the primary latch to the data output of the primary latch and at least one clock signal that latches data on the data input of a secondary latch to the data output of the secondary latch.

14. The integrated circuit of claim 9 further comprising a plurality of write ports on the data input of the primary latch.

15. The integrated circuit of claim 9 further comprising a plurality of read ports on the data output of the primary latch.

16. A method for performing a fast context switch in a register file, the method comprising the steps of:

(A) providing a register file bit that stores first and second bit values;

(B) when a context switch is required, swapping the first and second bit values.

17. The method of claim 16 wherein the swapping of the first and second bit values occurs in a single clock cycle.

18. The method of claim 16 wherein the register file bit comprises a first latch that stores the first value and a second latch that stores the second value, the first latch including a plurality of write ports and a plurality of read ports, the register file bit further including a feedback path that allows the first and second bit values in the first and second latches to be swapped.

19. A method for performing a fast context switch in a register file, the method comprising the steps of:

(A) storing a first value in a first latch of the register file;

(B) moving the first value in the first latch to a second latch;

(C) storing a second value in the first latch of the register file; and

(D) activating a context switch signal that causes the second value in the first latch to be stored in the second latch, and that causes the first value in the second latch to be stored in the first latch.

20. The method of claim 19 wherein the activation of the context switch signal in step (D) causes the context switch to occur in a single clock cycle.

21. A method for performing a fast context switch in a register file that includes a primary latch and a plurality of secondary latched, the method comprising the steps of:

(A) for each of the plurality of secondary latches, performing the steps of:

(A1) storing a value in the primary latch that corresponds to a selected thread;

(A2) moving the value in the primary latch to a secondary latch;

(B) storing a value in the primary latch that corresponds to an active thread;

(C) selecting one of the secondary latches for performing a context switch with the primary latch; and

(D) performing a context switch between the primary latch and the selected one secondary latch that causes the value in the primary latch to be stored in the selected one secondary latch, and that causes the value in the selected one secondary latch to be stored in the primary latch.

22. The method of claim 21 wherein the context switch performed in step (D) occurs in a single clock cycle.

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